Electronic Version
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Claims

[c1] A method of generating patterns of a paired set of photomasks from a data set defining a circuit layout to be provided on a substrate, comprising:
inputting a circuit layout;
identifying critical segments of said circuit layout;
generating and legalizing block mask patterns based on said identified critical segments; and
generating, legalizing and coloring phase mask patterns for use in a dual exposure method with said legalized block mask patterns,
wherein said legalized block mask patterns define a block mask and said colored legalized phase mask patterns define an alternating phase shift mask, said block mask and said alternating phase shift mask operable to be used together in a dual exposure method for patterning critical dimensioned features on said substrate.

[c2] The method of claim 1, wherein said method is performed using a processor.

[c3] The method of claim 2 further comprising generating data representing said legalized block mask patterns and said colored legalized phase mask patterns, and using

said generated data to fabricate said block mask and said phase-shifting mask, respectively.

[c4] The method of claim 3, further comprising checking for any violation of mask design rules prior to said step of generating said data.

[c5] The method of claim 4, further comprising modifying said circuit layout if there is a violation of said mask design rules, and performing again, in order, said steps of identifying critical segments, generating and legalizing block mask patterns, and generating, legalizing and coloring phase mask patterns.

[c6] The method of claim 1 wherein said phase mask patterns include pairs of juxtaposed etched regions in said phase mask, each region of each said pair having a pathlength difference of an odd number of half wavelengths relative to the other region of each said pair.

[c7] A computer readable medium including a set of instructions recorded thereon for performing a method of generating patterns of a paired set of photomasks from a data set defining a circuit layout to be provided on a substrate, said method comprising:
inputting a circuit layout;
identifying critical segments of said circuit layout;

generating and legalizing block mask patterns based on said identified critical segments; and

generating, legalizing and coloring phase mask patterns for use in a dual exposure method with said legalized block mask patterns,

wherein said legalized block mask patterns define a block mask and said colored legalized phase mask patterns define an alternating phase shift mask, said block mask and said alternating phase shift mask operable to be used together in a dual exposure method for patterning critical dimensioned features on said substrate.

[c8] The computer readable medium of claim 7 wherein said method is adapted to be performed using a processor.

[c9] The computer readable medium of claim 8 wherein said method further comprises generating data representing said legalized block mask patterns and said colored legalized phase mask patterns, and using said generated data to fabricate said block mask and said phase-shifting mask, respectively.

[c10] The computer readable medium of claim 9 wherein said method further comprises checking for any violation of mask design rules prior to said step of generating said data.

[c11] The computer readable medium of claim 10 wherein said method further comprises modifying said circuit layout if there is a violation of said mask design rules, and performing again, in order, said steps of identifying critical segments, generating and legalizing block mask patterns, and generating, legalizing and coloring phase mask patterns.

[c12] The computer readable medium of claim 7 wherein said phase mask patterns include pairs of juxtaposed etched regions in said phase mask, each region of each said pair having a pathlength difference of an odd number of half wavelengths relative to the other region of each said pair.

[c13] An apparatus for generating patterns of a paired set of photomasks from a data set defining a circuit layout to be provided on a substrate, comprising:
a processor; and
an input output (IO) interface connected to said processor,
said processor being operable to input a circuit layout over said
IO interface, to identify critical segments of said circuit layout, to generate and legalize block mask patterns based on said identified critical segments, and to thereafter generate, legalize and color phase mask patterns

for use in a dual exposure method with said legalized block mask patterns,
wherein said legalized block mask patterns define a block mask and said colored legalized phase mask patterns define an alternating phase shift mask, said block mask and said alternating phase shift mask operable to be used together in a dual exposure method for patterning critical dimensioned features on said substrate.

[c14] The apparatus of claim 13, wherein said processor is further operable to generate data representing said legalized block mask patterns and said colored legalized phase mask patterns for use in fabricating said block mask and said phase-shifting mask, respectively.

[c15] The apparatus of claim 14, wherein said processor is further operable to check for any violation of mask design rules prior to generating said data.

[c16] The apparatus of claim 15, further wherein said processor is further operable to modify said circuit layout if there is a violation of said mask design rules, and to identify critical segments, generate and legalize block mask patterns, and generate, legalize and color phase mask patterns again, in order.

[c17] The apparatus of claim 13 wherein said phase mask pat-

terns include pairs of juxtaposed etched regions in said phase mask, each region of each said pair having a path-length difference of an odd number of half wavelengths relative to the other region of each said pair.